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01/26/99

Class Subclass

ISSUE CLASSIFICATION

SCANNED

PROVISIONAL  
APPLICATION  
NUMBER

60117186

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Mailed

1. Application \_\_\_\_\_ papers.

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PATENT APPLICATION SERIAL NO. \_\_\_\_\_

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
Fee Record Sheet

1/1999 SCHAPMAN 00000054 122325 60117186  
1:114 150.00 CH

PTO-1556

(5/87)

\*U.S. GPO: 1988-433-214/80404

SERIAL NUMBER  60/117,186 PROVISIONAL	FILING DATE  01/26/99	CLASS	GROUP ART UNIT  0000	ATTORNEY DOCKET NO.  1-17
------------------------------------------------	-----------------------------	-------	----------------------------	---------------------------------

APPLICANT  
MAHJOUR ALI ABDELGADIR, ORLANDO, FL; GLENN B. ALERS, CHATHAM, NJ;  
JOSEPH WILLIAM BUCKFELLER, ALLENTOWN, PA; JEFFREY DEVIN BUDE,  
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WONG, SUMMIT, NJ; SUSAN M. ZAHURAK, LEBANON, PA.

\*\*CONTINUING DOMESTIC DATA\*\*\*\*\*  
VERIFIED

\*\*371 (NAT'L STAGE) DATA\*\*\*\*\*  
VERIFIED

\*\*FOREIGN APPLICATIONS\*\*\*\*\*  
VERIFIED

FOREIGN FILING LICENSE GRANTED 02/22/99

Foreign Priority claimed 35 USC 119 (e-d) conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY FL	SHEETS DRAWING 0	TOTAL CLAIMS	INDEPENDENT CLAIMS
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Verified and Acknowledged  
Examiner's Initials \_\_\_\_\_ Initials \_\_\_\_\_

DOCKET ADMINISTRATOR ROOM 3C 512  
LUCENT TECHNOLOGIES INC  
600 MOUNTAIN AVENUE  
P O BOX 636  
MURRAY HILL NJ 07974-0636

TITLE  
PLANARIZATION TECHNIQUE FOR HDPCVD FSG LAYER

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JC542 U.S. PTO  
01/26/99

Abdelgadir 1-17

IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

PROVISIONAL APPLICATION

Mahjoub Ali Abdelgadir  
Glenn B. Alers  
Joseph William Buckfeller  
Jeffrey Devin Bude  
Siddhartha Bhowmik  
Jane P. Chang  
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Isik C. Kizilyalli  
James Joseph Krajewski  
Michael Manfra  
Marco Mastrapasqua  
Alvaro Maury  
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Sailesh Mansinh Merchant

Donald Winslow Murphy  
Loren Neil Pfeiffer  
Michael Louis Steigerwald  
Hem M. Vaidya  
Kenneth William West  
Yiu-Huen Wong  
Susan M. Zahurak

Case: 1-17

Title: Planarization Technique For HDPCVD FSG Layer

COMMISSIONER OF PATENTS AND TRADEMARKS  
WASHINGTON, D. C. 20231

66/117186 PTO  
66/117186 PTO

PROVISIONAL APPLICATION COVER SHEET

SIR:

This is a request to file a Provisional Application under 37 CFR 1.53 (c).

[X] 25 number of pages in Specification

[ ] sheet(s) of drawing(s)

[ ] Assignment (this should appear on transmittal letter if the assignment is filed).

[ ] The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

No

Yes, the name of the U. S. Government agency and the Government contract numbers: \_\_\_\_\_

Inventor (s): (Full name and address)

1. Mahjour Ali Abdelgadir, 507 Fitzwilliam Way, Orlando, Florida 32828
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Yolanda W. Mikovits  
(Printed name of person mailing paper or fax)  
Yolanda W. Mikovits  
(Signature of person mailing paper or fax)

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23. Kenneth William West, 45 Corey Lane, Mendham, New Jersey 07945
24. Yiu-Huen Wong, 160 Woodland Avenue, Summit, New Jersey 07901
25. Susan M. Zahurak, RD #3, Box 1300 Boltz Lane, Lebanon, Pennsylvania 17046

Please file the application and charge Lucent Technologies Deposit Account No. 12-2325 the amount of \$150.00, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Deposit Account No. 12-2325 as required to correct the error.

Please address all correspondence to Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P. O. Box 636, Murray Hill, New Jersey 07974-0636. However, telephone calls should be made to me at 610-712-7955.

Respectfully,



Martin G. Meder  
Attorney for Applicant(s), Reg. No. 34674

Date: 1/26/99  
Lucent Technologies Inc.  
600 Mountain Avenue (Room 3C-512)  
P. O. Box 636  
Murray Hill, New Jersey 07974-0636

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address	IP LAW USE
Alvaro Maury	407-371-7523	DR-301C2338	538115000	maury@lucent.com	Design or Process Sess:
Mahjoub Abdalgadir	407-371-6592	DR-301C2192	538114000	mabdelgadir@lucent.com	Submission N : 117553
					Date Received:-
					Attorney:

**TITLE: "Planarization Technique for HDPCVD FSG Layer"**

Problem(s) addressed by the invention:

This invention addresses the problem of using HDPCVD FSG as a low k oxide between metal lines, without running the risk of exposing the metal to potential fluorine attack.

Closest known solution:

N/A

**DESCRIPTION OF THE INVENTION**, keyed to drawings, sketches, photographs, etc., sufficient to enable one knowledgeable

in the invention's field of technology to understand construction and operation of the invention.

**Summary (30 words or less):** The invention consists of depositing the gap fill HDPCVD FSG layer to a thickness at least 2500 Å higher than the metal thickness. This is followed by a short CMP step to partially reduce the high oxide peaks, and less at least 1000 Å on top of the metal. A second undoped dielectric is deposited, and completely planarized by CMP, if so required.

**Detailed Description:** Fig. 1 shows a cross-section of the metal level after the gapfill FSG deposition by HDPCVD. The thickness of oxide on top of metal will vary according to metal linewidth, with the wide lines (above a certain dimension) having the full oxide thickness. The wafer is then polished using high planarity conditions, to remove an equivalent blanket oxide thickness of about 1500 Å. This step reduces significantly the oxide peaks on top of metal, without exposing metal lines. State of the art CMP tools can produce this result consistently in a manufacturing environment. After the first CMP step, a second (undoped) oxide layer is deposited, and a second CMP step done to fully planarize the structure. If dummy fill patterns are used at metal photo, the second CMP step may not be necessary.

**Advantages:**

This technique allows the integration of a low k material without having to use a very thick FSG deposition (which is very expensive).

**Commercial product(s) or other applications in which the invention may be used:**

Any device manufactured by Lucent ME in which a low k ILD layer is required.

**Explain how use of the invention would be detected:**

SEM cross-sections would show whether this approach has been used.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

Alvaro Maury

date

M. A. Abdalgadir

date

This invention submission has been read and understood by the following two witnesses:

Jay Y. J. Lee

date

Adebanya

date

Planarization techniques for HDP CVD TiSi

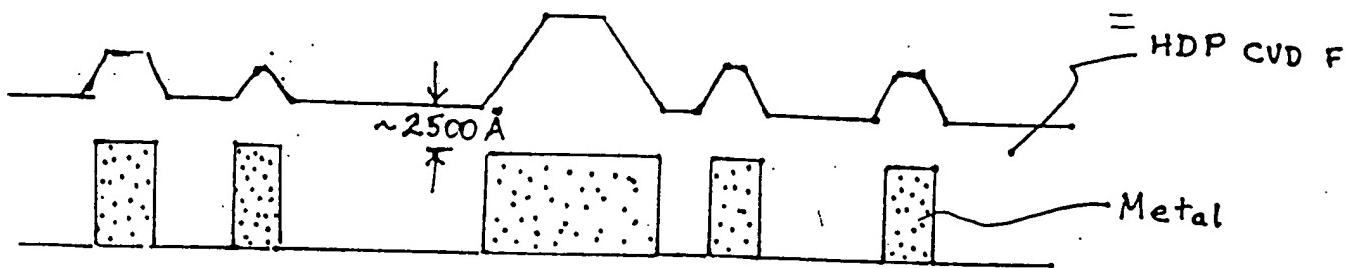


Fig. 1 - After HDP CVD FSG Deposition

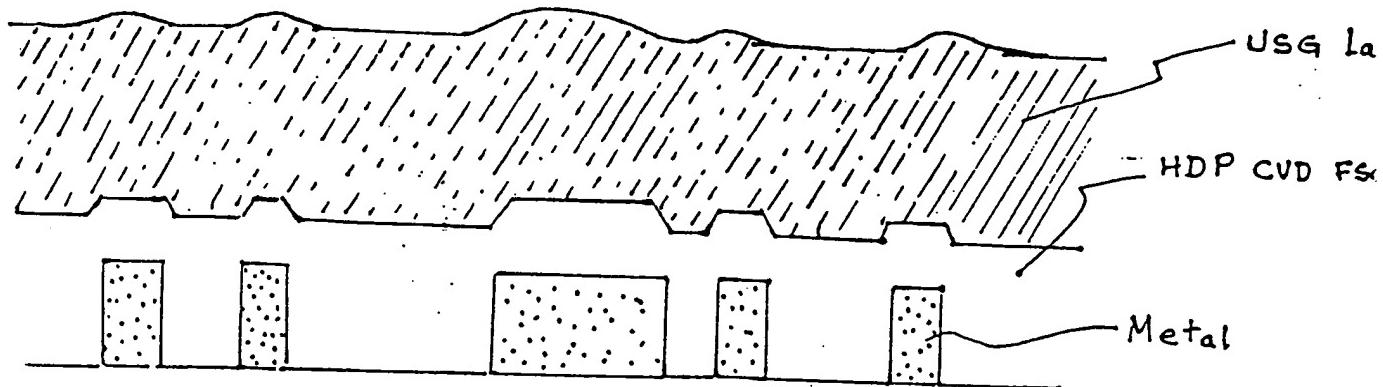


Fig. 2 - After short CMP step, and Undoped Oxide Deposition.

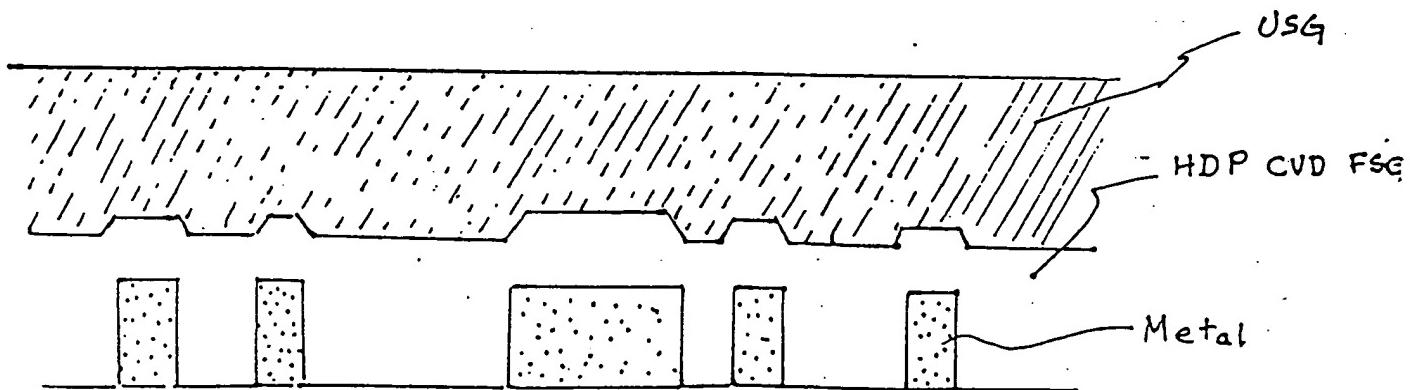


Fig. 3 - After Final CMP on USG Layer

## MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
I.C. Kizilyalli	407-371-7554	ED-219B	BL011122 A	ick@cmos
M. Mastrangelo	903-582-3408	20-319B	BL011124	mastrangelo@lucent.com

**TITLE:** Charge Injection Transistor Using High-K Dielectrics.

**IP LAW USE**

Submission No: 117554

Date Received: \_\_\_\_\_

Attorney: \_\_\_\_\_

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

**1. Describe the problem your invention solves:**

A silicon based negative-differential-resistance transistor is suggested that utilizes  $\text{SiO}_2/\text{Ta}_2\text{O}_5$  barrier layer.

**2. Based on information of which you are already aware, describe:**

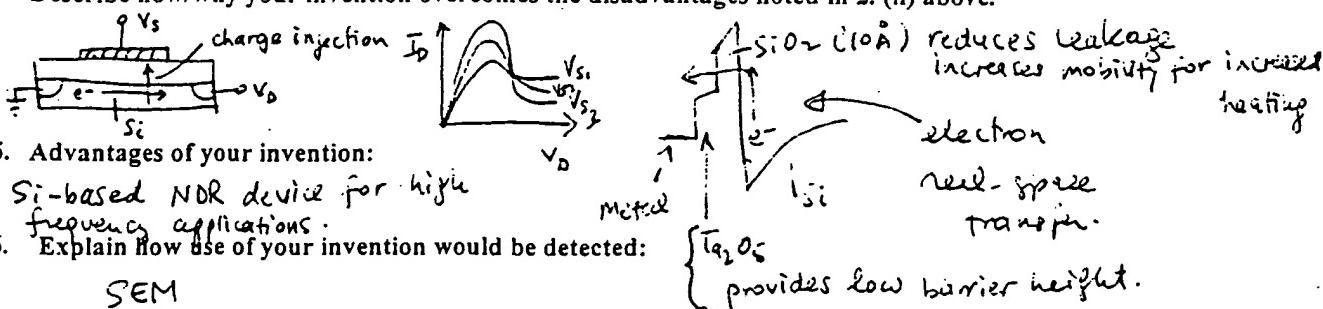
- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

- GaAs-based devices
- Large leakage currents
- Expensive

**3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:**

$\text{Si}/\text{SiO}_2$  (High-K dielectric) stack is used. Electrons are heated using the source-drain electric field. Charge injection into the poly (or metal) is modified by the S/D voltage. High-K dielectric provides low barrier height.

**4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.**



**5. Advantages of your invention:**

Si-based NDR device for high frequency applications.

**6. Explain how use of your invention would be detected:**

SEM

{ provides low barrier height.

**7.**

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

*I.C. Kizilyalli*

date

date

\_\_\_\_\_

date

date

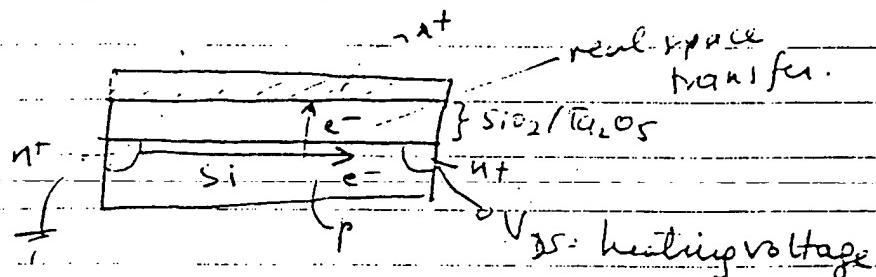
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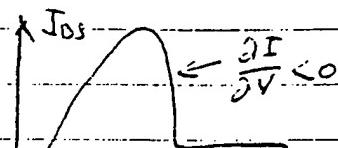
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## Charge Injection Transistor Using $Ta_2O_5$

Negative differential resistance is achieved through real space transfer of electrons from the Si channel through the  $SiO_2/Ta_2O_5$  gate into the n+ poly silicon substitute using the S-D voltage and substrate bias. The structure is similar to AlGaAs/GaAs CHINTs.



expected drain current  $I_{DS}$



$\frac{dI}{dV} < 0$  : Negative Differential Resistance

Useful for Si microwave devices

M. M. Vaidik

## MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Glenn B. Alers	(908) 582-4375	MH 3L-302	BL011114-	

**TITLE:** Sequential Anneal Process For Metal-Oxide-Metal Capacitors

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

<b>IP LAW USE</b>
Submission No: <u>117572</u>
Date Received: _____
Attorney: _____

1. Problems that is Addressed: Current low temperature anneal processes are not adequate for dielectric films greater than about 20nm.
2. Description of Current Practice: Metal-oxide films (such as tantalum oxide, titanium oxide, aluminum oxide...) can be used to form a capacitor with metal electrodes (such as TiN, TaN, WN, Al) for both sides. However, after deposition, the films must be annealed to improve the dielectric properties. High temperature anneals cannot be used with metal electrodes due to chemical reactions that occur between the electrode and the oxide layer which can decrease capacitance or increase leakage current. An alternate approach is to use a plasma of an oxygen containing gas to anneal the dielectric layer at temperatures less than ~400 C. However, ions from the plasma will not penetrate into the dielectric layer more than roughly 10-20nm. (SIMS data) Therefore, this anneal process is inadequate for films greater than 20nm.
3. Solution to Problem: For dielectric films greater than ~20nm, it is possible to deposit the film in 2-20nm intervals, each thickness interval is followed a plasma process to anneal the thinner film. In this way, films of any thickness can be grown and annealed at the low temperatures required for use with metal electrodes.
4. Present Commercial Practice: Metal oxide films with a thickness of 10nm or less are being used with poly-Si or SiN electrodes and a high temperature (greater than 600 C) anneal step.
5. Explain how use of your invention would be detected: Cluster tools might be marketed with a built in multi-step anneal process.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

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This invention submission has been read and understood by the following two witnesses:

date	date	date
date	date	date
date		

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Glenn B. Alers	(908) 582-4375	MH 3L-302	BL011114-	

**TITLE:** Capacitor With Thin Metal Electrodes

IP LAW USE  
Submission No: 117555  
Date Received: \_\_\_\_\_  
Attorney: \_\_\_\_\_

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

1. Problems that is Addressed: Excess surface roughness of the bottom electrode of a metal-oxide-metal capacitor can increase the leakage current for the capacitor.
  2. Description of Current Practice: Metal-oxide films (such as tantalum oxide, titanium oxide, aluminum oxide...) can be used to form a capacitor with metal electrodes (such as TiN, TaN, WN, Al) for both sides. To form such a structure, the use of a CVD deposited bottom electrode is desirable because of the enhanced step coverage properties of CVD allow 3 dimensional structures to be used for the capacitor with enhanced area. However, CVD films have a high surface roughness (AFM image). If this roughness is on the order of the film thickness, leakage currents are increased.
  3. Solution to Problem: The grain size of the CVD films can be reduced either by (1) Use very think CVD films less than about 20nm thick so that the morphology does not have a chance to form (2) Use a think PVD seed layer to seed smaller grain growth of the CVD film and therefore reduce roughness.
  4. Present Commercial Practice: Metal oxide films with a thickness of 10nm or less are being used with poly-Si or SiN electrodes and a high temperature (greater than 600 C) anneal step.
  5. Explain how use of your invention would be detected: If a cross section of the capacitor shows a metal layer less than 20nm (seed layer or complete layer) then there is a violation.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

**Submitter(s) signature(s) and date:**

This invention submission has been read and understood by the following two witnesses:

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# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Glenn B. Alers	(908) 582-4375	MH 3L-302	BL011114-	

**TITLE:** Capacitor With Tungsten Bottom Electrode

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

<b>IP LAW USE</b>
Submission No: <u>117557</u>
Date Received: _____
Attorney: _____

1. Problems that is Addressed: CVD deposition of metal oxide films (such as tantalum oxide, titanium oxide...) at temperatures higher than ~425 C can form tungsten oxide at the surface (WO<sub>x</sub> which is volatile and can lead to adhesion problems between the metal oxide film and the tungsten.
2. Solution to Problem: Any combination of the following processes can reduce this problems. (1) Deposit the metal oxide film at less than 425 C to prevent the formation of WO<sub>x</sub>. (2) Treat the tungsten surface to form WN before the metal oxide film is deposited. Possible treatments include plasma process in nitrogen or forming gas or RTA in ammonia.
3. Present Commercial Practice: Metal oxide films with a thickness of 10nm or less are being used with poly-Si or SiN electrodes and a high temperature (greater than 600 C) anneal step.
4. Explain how use of your invention would be detected: SIM analysis that shows the presence of WN at interface.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

\_\_\_\_\_  
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# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Glenn B. Alers	(908) 582-4375	MH 3L-302	BL011114-	

**TITLE:** Capacitor With Amorphous Metal-Oxide Dielectric

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

**IP LAW USE**  
 Submission No: 117558  
 Date Received:  
 Attorney:

1. Problems that is Addressed: Morphology change of dielectric layer.
2. Summary of Problem: Current DRAM processes use poly-Si/SiN electrodes with a high temperature anneal step that crystallizes the films. However, when the film crystallizes the surface roughness increases and pin-holes form in the dielectric which can lead to oxidation of the bottom electrode. This roughness increase also limits the minimum thickness of the dielectric film that can be used (one cannot have a thickness less than the roughness).
2. Solution to Problem: Use an amorphous instead of crystalline dielectric layer. If the post processing temperature is kept low then the film can remain amorphous. Alternatively, alloy elements of Al, Ti, Mo can increase the crystallization temperature of the tantalum oxide and will allow thinner films to be used.
3. Explain how use of your invention would be detected: HRTEM cross section analysis.

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\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

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This invention submission has been read and understood by the following two witnesses:

date

date

date

date

date

date

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Gregg Higashi	407-371-7646	CR/30-1 E2000	538113000	higashi@lucent.com

**TITLE:** W-Plug Anchor for High-K MOM Capacitors

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

IP LAW USE	
Submission No:	117559
Date Received:	
Attorney:	

1. Describe the problem your invention solves:

This invention keeps W-plugs from falling out during MOM capacitor processing.

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and  
(ii) the disadvantages of the previous attempts.

There are no other attempts to solve this particular problem that I am aware of.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

See attached

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

See attached

5. Advantages of your invention:

Higher capacitance, higher yield

6. Explain how use of your invention would be detected:

SEM cross-section

- 7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

Gregg Higashi

date

This invention submission has been read and understood by the following two witnesses:

Doris

date

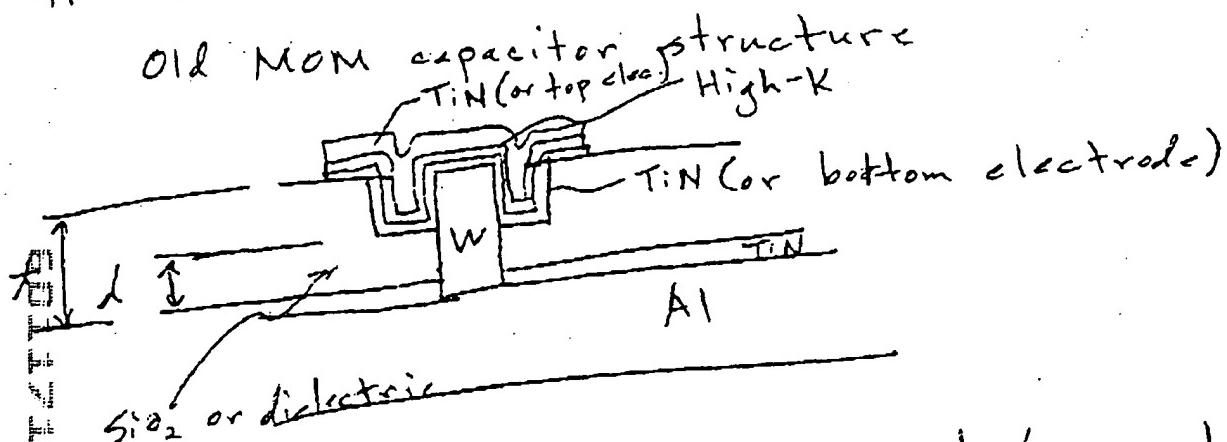
Patricia Kiley

date

### 3. Summary of invention.

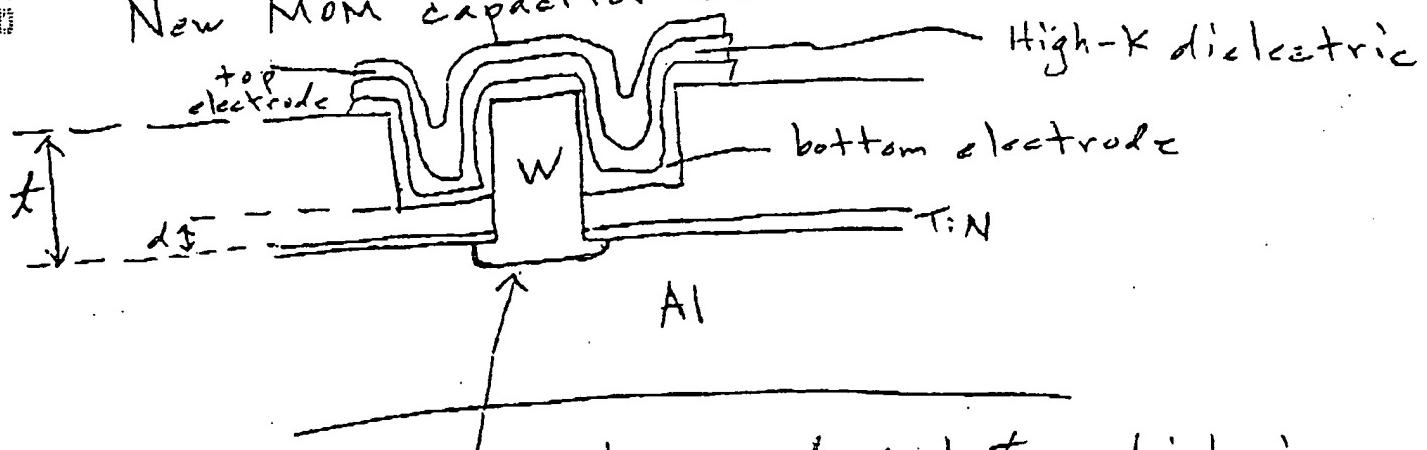
The recessed MOM capacitor structure is limited in depth, and therefore capacitance, by the lifting out of the W-plugs. W-plug anchors solve this problem.

### 4. Describe invention:



$d$  is typically limited to  $\frac{1}{2}t$ , where  $t$  is the thickness of the dielectric

### New MOM capacitor structure



W-plug anchor allows  $d < \frac{1}{2}t$  which increases the total capacitance of the bottom electrode, High-K dielectric, top electrode stack.

Old Process

Via Etch

Via Etch Clean

Barrier Dep

W-CVD

:

etc

New Process

Via Etch

Via Etch Clean

Isotropic Al etch

Barrier Dep  $\rightarrow$  (+ clean if needed)

W-CVD

:

etc

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Y. H. Wong	(408) 582-3919	MH TA-265	BLO 1131 FO	hyw@ust.hk
D. W. Murphy	(408) 582-2962	MH TA-263	BLO 1131 AO	dwm@ust.hk

TITLE: Fluorinated Aero-gel for low k Passivation

Important Note: Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

IP LAW USE  
Submission No: 117560  
Date Received: \_\_\_\_\_  
Attorney: \_\_\_\_\_

1. Describe the problem your invention solves:

Very low  $k$  dielectric

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Aero-gel normally is made based on Al<sup>3+</sup> chemistry. By replacing Al with F, it would be compatible with Cu metallization.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

Aero-gel with F chemistry will passivate Cu as well as Al, which are the metallization scheme for silicon IC. It also has  $k < 2$ .

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

5. Advantages of your invention:

Very low  $k$  and form very stable interface to Cu and Al.

6. Explain how use of your invention would be detected:

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date

date

date

date

date

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Y.H. Wong	(908)582-3779	MH 1A-265	RLO 1131FO	whywnt
L. Phifer	(908)582-2710	MH 7A-219	RLO 111710	tub
K. West	(908)582-2060	MH 7A-222	RLO 111710	kwu
M. Mangra	(908)582-1137	MH 1C-459	RLO 111710	mangra
TITLE: <u>Epi-AlN for gate dielectrics</u>				
<b>Important Note:</b> Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.				
<b>IP LAW USE</b> Submission No: <u>117561</u> Date Received: _____ Attorney: _____				

**1. Describe the problem your invention solves:**

Low interface states, high  $k$  ( $\sim 10$ ) and good diffusion barrier to  
B, P, etc.

**2. Based on information of which you are already aware, describe:**

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Good ~~Si~~ lattice match to Si with epitaxial AlN will lower the interface state density and allow better control, therefore  $\Delta V_{th}$ .

**3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:**

Grow epitaxial AlN on Si by MBE or any other technique.

**4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.**

**5. Advantages of your invention:**

See 1.

**6. Explain how use of your invention would be detected:**

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date	date
date	date
date	date

# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
M. Steigenswald	(908) 582-7491			
Y.H. Wong	(908) 582-3979	MH 1A - 265	B1n131FO	Whynot
R.M. Fleming	(908) 582-7491	MH 1D-345	BL01131AO	mls

S. Takanishi  
TITLE: PVD of high k with C- and N-based gases

Jane Cheung  
**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

IP LAW USE	
Submission No:	117562
Date Received:	
Attorney:	

**1. Describe the problem your invention solves:**

Create carbide and/or nitride interface in-situ between high k films and electrodes.

**2. Based on information of which you are already aware, describe:**

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Besides the interface, films doped with carbon and nitrogen tend to have lower leakage and better electrical performance.

**3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:**

**4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.**

**5. Advantages of your invention:**

Carbon and nitrogen interface in-situ film graded doping.

**6. Explain how use of your invention would be detected:**

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

/ date

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/ date

/ date

/ date

/ date

# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
J. Bude	(408)582-3615	MH 2D-307B	BL0111250	bude
S. Merchant				
Y.H. Wong	(408)582-3979	MH 1A-265	BL01131FO	WhyNot
P. Dippold				

TITLE: Multi-use MOM

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

IP LAW USE
Submission No: <u>117564</u>
Date Received: _____
Attorney: _____

1. Describe the problem your invention solves:

Generalized MOM platform for memories, such as SRAM, DRAM,

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Flash, FeRAM .. even magnetic .

Integrate all the memory functions by appropriate processing and minimum processing steps.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

High k thin film with the appropriate electrical performance in combination w/wo other dielectric to form MOM capacitors.

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

Standard mom structure.

5. Advantages of your invention:

Simplicity in design and process, yet flexible in system configuration.

6. Explain how use of your invention would be detected:

SEM's

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date	date
date	date
date	date

## MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
S. Merchant				
Y.H. Wong	(408) 582-3919	MH 1A-265	BLD 113 (FO)	whynot
M. Stegerwald	(408) 582-7461	MH 1B-345	BLO 113/AO	mks

**TITLE:** New Geometry Structure / Cu Plug

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

<b>IP LAW USE</b>
Submission No: <u>117565</u>
Date Received: _____
Attorney: _____

**1. Describe the problem your invention solves:**

Enhance the surface area of Cu plug for higher specific capacitance therefore higher density.

**2. Based on information of which you are already aware, describe:**

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Cu plugs have different structural morphology as compared to Ti and Al. Similar method but different chemistry is needed

**3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:**

Higher density MOM in Cu metallization.

**4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.**

**5. Advantages of your invention:**

Higher density memory.

**6. Explain how use of your invention would be detected:**

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

**Submitter(s) signature(s) and date:**

**This invention submission has been read and understood by the following two witnesses:**

date

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date

date

date

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Y.H. Wong	(908)582-3979	MH 1A-265	BLO 1131 FO	WhyNot
M. Steigenswal	(908)582-7491	MH 1D-345	BLO 1131 AO	M/S
S. Merchant	7			

→ M. Mader  
TITLE: F-passivation of Cu

<b>IP LAW USE</b>
Submission No: <u>117567</u>
Date Received: _____
Attorney: _____

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

**1. Describe the problem your invention solves:**

Establish a stable Cu surface for subsequent processing of Cu interconnect.

**2. Based on information of which you are already aware, describe:**

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

$\text{CuF}_2$  is extremely stable. We propose ways to achieve it.

A.V.C (CuF A.R.E)

**3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:**

Ion implantation, plasma treatment and/or electrochemically treating the Cu with F containing and active species.

**4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.**

**5. Advantages of your invention:**

Take full advantage of Cu chemistry.

**6. Explain how use of your invention would be detected:**

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s), signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date

date

date

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date

date

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

Name(s) of Submitters	Telephone N :	Loc/Room	Organization	E-Mail Address
Y.H. Wong	(908)582-3919	MH 1A-265	BLD 1131FO	whynot
M. Skoglund				
S. Merchant	(908)582-7491	MH 1D-345	BLD 1131AO	mjs@pent.ca

**TITLE:** Surface Modification of Metal Surface  
*Recessed*

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

<b>IP LAW USE</b>
Submission No: <u>117568</u>
Date Received: _____
Attorney: _____

1. Describe the problem your invention solves:

*Create barrier layer on metal based on the intrinsic chemistry of metal*

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and  
(ii) the disadvantages of the previous attempts.

*Deposit and form with extrinsic film the barrier layer*

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

*With techniques such ion implantation, ion sputtering w/w/o plasma or chemical treatment (can be electrochemically), inert metal surface results.*

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

5. Advantages of your invention:

*Utilize the properties of the metal to take care of the interface and interdiffusion issues.*

6. Explain how use of your invention would be detected:

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date

date

date

date

date

date

# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Y.H. Wong	(908)582-3979	MH 1A - 265	BLO 1131FO	whynot
S. Merchant				
M. Steigenswald	(908)582-7491	MH 1D-345	BLO 1131AO	m/s@lucent.com
M. Meden				

→ TITLE: Encapsulation of Cu with F-glass

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

<u>IP LAW USE</u>	
Submission No:	117569
Date Received:	
Attorney:	

1. Describe the problem your invention solves:

Passivate the surface of Cu thin films.

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

Since  $CuF_2$  is extremely stable and have a strong chemical bond, stable fluorinated glass should be a good match.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

Similar to SiNH encapsulation for IC device with Cu interconnect, F-glass is suitable.

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

5. Advantages of your invention:

$CuF_2$  is at least as stable if not better than  $Cu_xSi_y$  or  $Cu_xNy$  bonds in Cu encapsulated in SiNH film.

6. Explain how use of your invention would be detected:

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

date

date

date

date

date

date

# MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION

Name(s) of Submitters	Telephone No:	Loc/Room	Organization	E-Mail Address
Y.H. Wong	(408)582-3979	MH 1A-265	BLO 1131FO	Whynot
M. Steigenswald	(408)582-7449	MUT 1D-345	BLO 1131FO	M/S
J. Krajewski	408 582 2629	MH 1A 374	BLO 1131FO	JJKeluent.com
S. Zalczak	(408)582 3763	MH 1A 176	BLO 1131FO	57

TITLE: Microwave CVD ~~higher quality CVD films~~

<b>IP LAW USE</b>
Submission No: <u>117570</u>
Date Received: _____
Attorney: _____

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple.

1. Describe the problem your invention solves:

*Higher quality CVD films*

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

*Presently CVD films need post-deposition annealing. Microwave plasma is one way to do it. The present technique encompasses both in-situ.*

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

*It allows in-situ control of gas phase kinetics in the deposition and subsequently treatment of the film.*

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

*Standard CVD chamber with downstream and/or immersed microwave plasma.*

5. Advantages of your invention:

*Surface preparation, bias and cleanliness.*

6. Explain how use of your invention would be detected:

7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

*Y-H Wong*

This invention submission has been read and understood by the following two witnesses:

*[Signature]*

date

date

date

date

date

**MICROELECTRONICS PATENT COMMITTEE INVENTION SUBMISSION**

SUNDAR CHOUR 407-371-6788 301C-1090 538162000 *et al/luv@luce.com*  
 Name(s) of Submitters Telephone No: Loc/Room Organization E-Mail Address  
 PHIL DODATO 908-582-5569 2D-325 BLD 111240 PWD@Lucent.com  
 HEM VADIA 407-371-6646 301W-2208 BLD 111280 *hem@lucent.com*  
 JAMES T. CLEMENS 908-582-2800 BLD 111280 *Jtcleme@lucent.com*

ALVARO MARY 407-371-7523 301C-2331 S38115000 *IP LAW USE*  
 TITLE: Integration Capacitor in dual damascene architecture

**Important Note:** Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist.

Avoid the use of undefined acronyms and jargon. Keep the language simple.

Submission No: 117571

Date Received:

Attorney:

1. Describe the problem your invention solves:

*Increases Capacitor plate area, without increasing memory cell area -*

2. Based on information of which you are already aware, describe:

- (i) previous attempts to solve the problem your invention solves; and
- (ii) the disadvantages of the previous attempts.

*In past interlevel dielectric etch back was used to increase surface area of mem capacitor-*

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

*Please see attached page which describes process flow for new structure -*

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

5. Advantages of your invention: Due to increase in surface capacity area, other parameters such as thickness of Ta2O5 + speed can be relaxed.

6. Explain how use of your invention would be detected:

*Cross section, TEM, SEM*

- 7.

\*\*\* Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc. \*\*\*

Submitter(s) signature(s) and date:

This invention submission has been read and understood by the following two witnesses:

*Phil Dodato*

date

date

*Hem Vadia*

date

date

*James Clemens*

date

date

*Alvaro Mary*

date

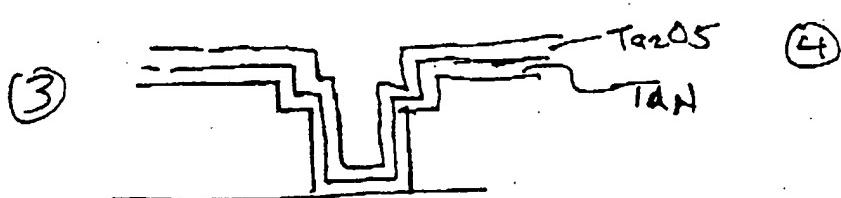
date



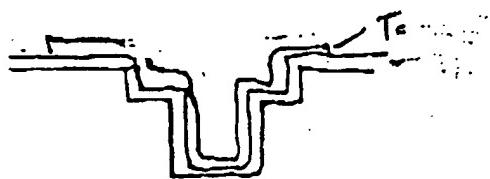
②



Pattern 3<sup>rd</sup> ETCH  
D1 for Dual-Dam  
for Interconnect

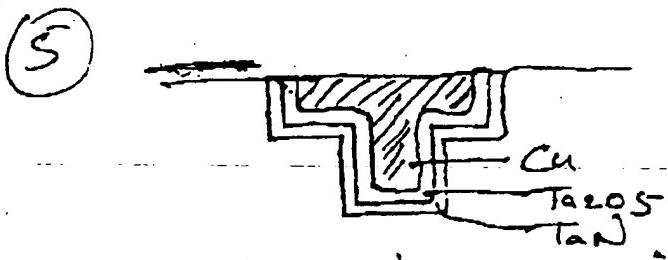


④



Dep. TiN (Barrier) + Ta<sub>2</sub>O<sub>5</sub>

Pattern 5<sup>th</sup> ETCH Ti



⑥

SPECIAL CLEANING  
Remove metal Dep.  
for Ta<sub>2</sub>O<sub>5</sub> Inter.

Dep.Cu 3<sup>rd</sup> CMP

22

PROJECT NAME

Submission: 117520 NOTEBOOK NO.

1-15-99

Atty: Martin G. Sander

Buckfeller

De Carter in RF chamber

Brownmiller

TO GO IN CONVERSATION WITH merchant

markman

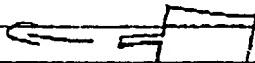
PATENT # 116,769 - Defect Density

Control For RF ETCH CHAMBERS

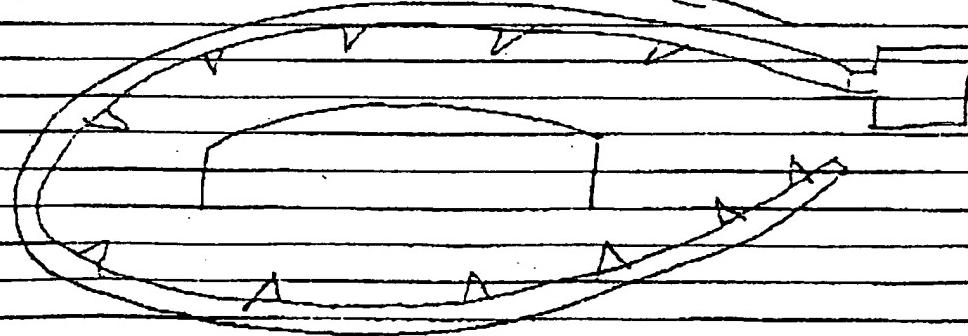
- (1) INSTALL SPIDER GAS DELIVERY SYSTEM TO  
P2 MODULE ON NOVELLUS EQUIPMENT. THIS  
WILL ALLOW UNIFORM DISTRIBUTION OF THE  
AXIAL GAS FOR RF ETCH. DRAWING BELOW

Current

GAS IN



PROPOSED

Top/Bottom  
GAS Delivery

Page 1 of 2

SIGNATURE

READ AND UNDERSTOOD

DATE

19

DATE

19

23

PROJECT NAME \_\_\_\_\_

NOTEBOOK NO. \_\_\_\_\_

CONTRIBUTORS

Joseph W Buckleher

Joseph W Buckleher  
1-15-99DavidShawn  
1/15/99Read and UnderstoodAgreeSIGNATURE \_\_\_\_\_  
READ AND UNDERSTOOD \_\_\_\_\_DATE 19  
DATE 19

**What is Claimed:**

- 1        1. An integrated circuit and process for making an integrated circuit,
- 2        substantially as shown and described herein.

0101100100000000

## REQUEST FOR ACCESS TO AN ABANDONED APPLICATION UNDER 37 CFR 1.14

In re Application of

Application Number

60/117,186

Filed

1-26-99

Paper No. *[Signature]*

I hereby request access under 37 CFR 1.14(a)(1)(iv) to the application file record of the above-identified ABANDONED application, which is identified in, or to which a benefit is claimed, in the following document (as shown in the attachment):

United States Patent Application Publication No. \_\_\_\_\_, page, \_\_\_\_\_ line \_\_\_\_\_.

United States Patent Number *6495409*, column \_\_\_\_\_, line, \_\_\_\_\_ or

WIPO Pub. No. \_\_\_\_\_, page \_\_\_\_\_, line \_\_\_\_\_.

**Related Information about Access to Pending Applications (37 CFR 1.14):**

Direct access to pending applications is not available to the public but copies may be available and may be purchased from the Office of Public Records upon payment of the appropriate fee (37 CFR 1.19(b)), as follows:

For published applications that are still pending, a member of the public may obtain a copy of:

- the file contents;
- the pending application as originally filed; or
- any document in the file of the pending application.

For unpublished applications that are still pending:

- (1) If the benefit of the pending application is claimed under 35 U.S.C. 119(e), 120, 121, or 365 in another application that has: (a) issued as a U.S. patent, or (b) published as a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of:
  - the file contents;
  - the pending application as originally filed; or
  - any document in the file of the pending application.
- (2) If the application is incorporated by reference or otherwise identified in a U.S. patent, a statutory invention registration, a U.S. patent application publication, or an international patent application publication in accordance with PCT Article 21(2), a member of the public may obtain a copy of:
  - the pending application as originally filed.

*S. Chan*

Signature

*S. Chan*

Typed or printed name

Registration Number, if applicable

Telephone Number

*Oct. 22, '03*

Date

PRO	
FOR PTO USE ONLY	
OCT 22 2003	
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(12) **United States Patent**  
Manfra et al.

(10) Patent No.: **US 6,495,409 B1**  
(45) Date of Patent: **Dec. 17, 2002**

(54) **MOS TRANSISTOR HAVING ALUMINUM NITRIDE GATE STRUCTURE AND METHOD OF MANUFACTURING SAME**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/472,331

(22) Filed: Dec. 23, 1999

**Related U.S. Application Data**

(60) Provisional application No. 60/117,186, filed on Jan. 26, 1999.

(51) Int. Cl.<sup>7</sup> ..... H01L 21/8238; H01L 29/76

(52) U.S. Cl. ..... 438/216; 438/261; 438/591; 438/240; 438/585; 257/410; 257/324

(58) Field of Search ..... 438/216, 261, 438/180, 46, 585; 257/315; 117/84, 204

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(57) **ABSTRACT**

An MOS transistor comprising a substrate, a source, a drain, and a gate, wherein the gate comprises aluminum nitride. Aluminum nitride is epitaxially grown on the silicon substrate at a substrate temperature of about 600° C. and subsequently annealed at a substrate temperature of about 950° C.

30 Claims, 1 Drawing Sheet

